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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,606	08/25/2003	S. Brandon Keller	100111233-1	2818

22879 7590 05/05/2006

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,606	KELLER ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/647,606 and appeal brief filed on 2/17/2006. Claims 1-17 remain pending in the application.

2. In view of the appeal brief filed on 2/17/06, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being obvious over Regnier (US 2003/0208721 A1).

5. As to claim 1, Regnier teaches a substantially hierarchical netlist (data structure) for a hierarchical circuit as shown in Fig. 1 (Fig. 3b-3d show such data structure) for use by a computer system (Fig. 2). The hierarchical netlist data structure comprises cells (hierarchical blocks) including cell names, cell instances (block instances) including cell instance names, ports (port instances) including port names or port instance names, nets including net names, and markers (Figs. 1, 3b-3d, see 0036-0043 for detail description). The ports (port instances) are used to connect from top level block(s) to lower level block(s) of the hierarchical netlist, where the ports are connected by nets. As shown in Fig. 1, each block comprises a plurality of instances connected by nets through each of the ports (port instances). The hierarchical netlist data is stored on computer storage medium. The stored hierarchical netlist data is used by ERC, LVS programs or other fault analysis systems (verification programs) to identify design errors or potential circuit faults through a search engine (0045, 0046). The verification programs must include connection check between components in order to verify there is any design error or potential circuit faults. The verification programs must include an error message or a warning indication during verification check. Note that the search engine loop through each port within the hierarchical netlist (at least see 0064-0066, 0071-0072). The "if" step as recited is well known to practitioners at the time the invention was made and commonly used by practitioners in the art in order to verify any design errors or potential circuit faults in a circuit design. Thus connection check as recited in the claim is within the scope of this application publication and would have been obvious to practitioners in the art at the time the invention was made because by

looping or traversing hierarchically through each port, connection error must be detected and a warning must be issued at specific location detected using the hierarchical netlist as taught by Regnier.

6. As to claim 2, Regnier teach the hierarchical netlist data is used by ERC, LVS programs or other fault analysis systems (verification programs) to identify design errors or potential circuit faults through a search engine (0045, 0046). Regnier teaches the verification programs are designed to search out critical or fault data, then perform analysis on the data (0046).

7. As to claim 3, a computer system (Fig. 2) operable by a designer (user). In order to fix or repair the detected error, a warning message must be transmitted to a user terminal.

8. As to claim 4, Fig. 1 shows a substantial identical hierarchical netlist (data structure) comprising a top hierarchical level of one of the hierarchical blocks that include a plurality of instances. Regnier teaches that the verification programs are designed to search out critical or fault data; then perform analysis on the data. In order to perform such searching, a top hierarchical level of one of the hierarchical blocks must be selected as an initial hierarchical block in the traversing step. For example, top 2 is selected as an initial hierarchical block in the traversing step. Note that Fig. 1 is for illustration, complex circuit may be found (see 6,886,140, Fig. 1).

9. As to claims 5-6 and 7-9, rejections set forth in claims 1-4 apply because the claimed limitations are substantially the same.

10. As to claims 10-12 and 13-16, rejections set forth in claims 1-4 also apply because the claimed limitations are substantially the same. Fig. 2 shows a computer system for use to detect design errors and other circuit faults during verification by ERC, LVS programs and other analysis systems (0044, 0046).

11. As to claims 17, rejections set forth in claims 1-4 apply because the claimed limitations are substantially the same. Regnier teaches a software product for identifying design errors and other faults in a circuit design and this software product is stored on a computer readable medium (0044, 0046).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

JACK CHIANG
SUPERVISORY PATENT EXAMINER

VUTHE SIEK
PRIMARY EXAMINER